Specification for Approval

Customer:_____

Model Name:_____

Supplier Approval			Customer approval
R&D Designed	R&D Approved	QC Approved	
Peter	Peng Jun		

Revision Record

REV NO.	REV DATE	CONTENTS	Note
A	2014-04-28	NEW ISSUE	
B	2018-09-05	MODIFY VIEWING	

Table of Contents

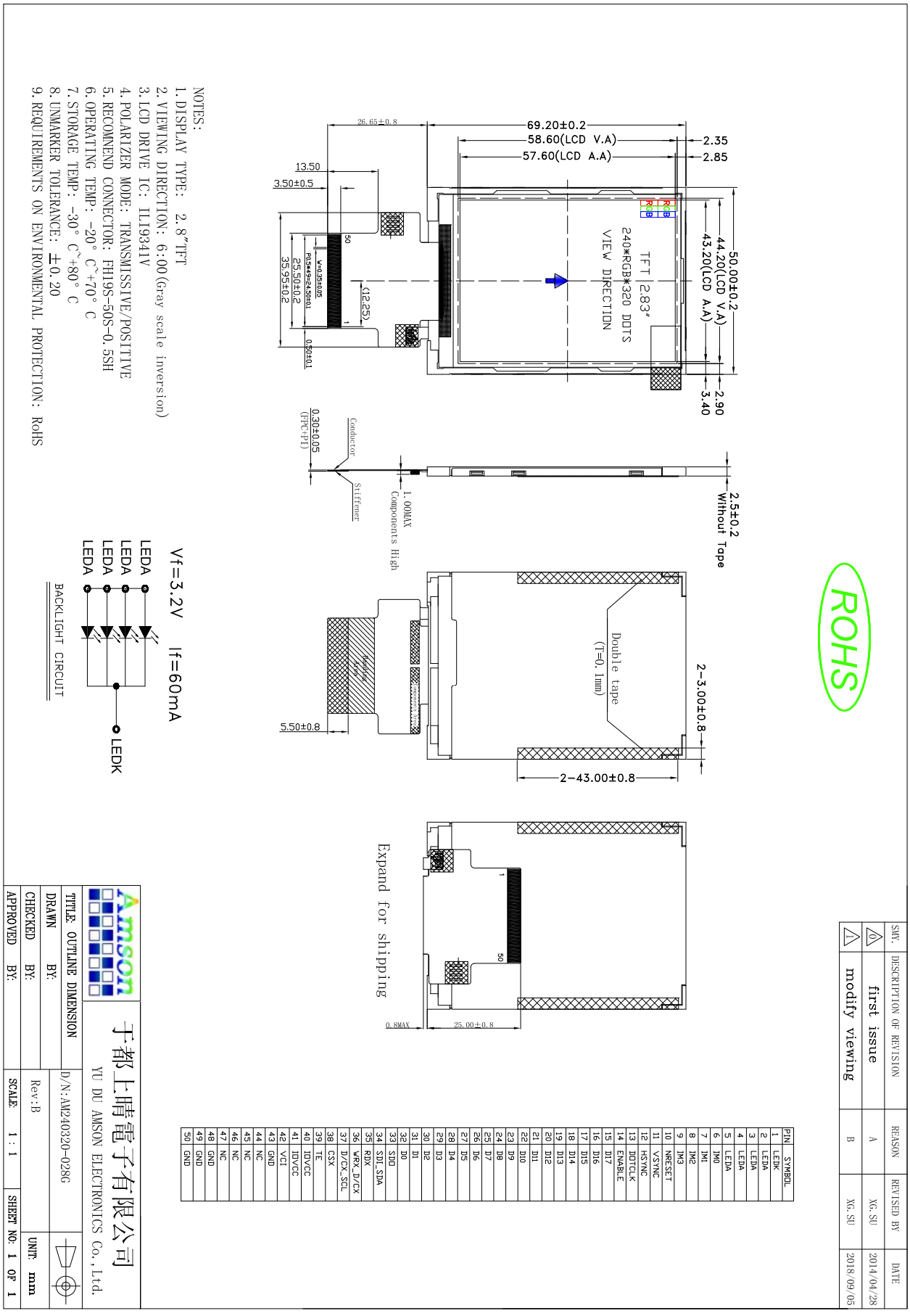
1. Scope

This specification defines general provisions as well as inspection standards for TFT module supplied by AMSON electronics.
If the event of unforeseen problem or unspecified items may occur, naturally shall negotiate and agree to solution.

2. General Information

ITEM	STANDARD VALUES	UNITS
LCD type	2.8”TFT	--
Dot arrangement	240(RGB)×320	dots
Color filter array	RGB vertical stripe	--
Display mode	TN / Transmission / Normally White	--
Viewing Direction	6 o’clock(Gray scale inversion)	--
Eyes Viewing Direction	12 O’clock	--
Driver IC	ILI9341V	--
Module size	50.0(W)×69.2(H)×2.5(T)	mm
Active area	43.2(W)×57.6(H)	mm
Dot pitch	0.18(W)×0.18(H)	mm
Interface	4-lines_8bit / 3-lines_9bit SPI 8-/ 9-/16-/18-bit 8080-series system interface 6-/16-/18-bit RGB interface	--
Operating temperature	-20 ~ +70	°C
Storage temperature	-30 ~ +80	°C
Back Light	4 White LED In Parallel	--
Weight	TBD	g

3. External Dimensions



PIN	SYMBOL
1	LEDK
2	LEDA
3	LEDA
4	LEDA
5	LEDA
6	IM0
7	IM1
8	IM2
9	IM3
10	NRESET
11	VSYNC
12	HSYNC
13	DOTCLK
14	ENABLE
15	D17
16	D16
17	D15
18	D14
19	D13
20	D12
21	D11
22	D10
23	D9
24	D8
25	D7
26	D6
27	D5
28	D4
29	D3
30	D2
31	D1
32	D0
33	SDO
34	SDI_SDA
35	RDX
36	WRX_D/CX
37	D/CX_SCL
38	CSX
39	TE
40	IOVCC
41	IOVCC
42	VCI
43	GND
44	NC
45	NC
46	NC
47	NC
48	GND
49	GND
50	GND

SMY.	DESCRIPTION OF REVISION	REASON	REVISED BY	DATE
1	modify viewing	B	XG. SU	2018/09/05
0	first issue	A	XG. SU	2014/04/28

TITLE: OUTLINE DIMENSION	D/N:AM240320-028G
DRAWN BY:	Rev:B
CHECKED BY:	UNIT: mm
APPROVED BY:	SCALE: 1 : 1 SHEET NO: 1 OF 1

宇都上晴電子有限公司
YU DU AMSON ELECTRONICS Co., Ltd.

4. Interface Description

<table>
<tr><th>Pin</th><th>Symbol</th><th>Description.</th></tr>
<tr><td>1</td><td>LEDK</td><td>LED backlight (Cathode).</td></tr>
<tr><td>2</td><td>LEDA</td><td>LED backlight (Anode).</td></tr>
<tr><td>3</td><td>LEDA</td><td>LED backlight (Anode).</td></tr>
<tr><td>4</td><td>LEDA</td><td>LED backlight (Anode).</td></tr>
<tr><td>5</td><td>LEDA</td><td>LED backlight (Anode).</td></tr>
<tr><td>6
7
8
9</td><td>IM0
IM1
IM2
IM3</td><td>System interface Mode
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface mode</th><th>DB Pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>i80-system 8-bit interface Ⅰ</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>i80-system 16-bit interface Ⅰ</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>i80-system 9-bit interface Ⅰ</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>i80-system 18-bit interface Ⅰ</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-wires_9-bit SPI Ⅰ</td><td>CSX,SDA,SCL</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-wires_8-bit SPI Ⅰ</td><td>CSX,RS,SDA,SCL</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>i80-system 16-bit interface Ⅱ</td><td>DB[17:10],DB[8:1]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>i80-system 8-bit interface Ⅱ</td><td>DB[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>i80-system 18-bit interface Ⅱ</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>i80-system 9-bit interface Ⅱ</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wires_9-bit SPI Ⅱ</td><td>CSX,SDI,SDO,SCL</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wires_8-bit SPI Ⅱ</td><td>CSX,D/CX,SDI,SDO,SCL</td></tr>
</table></td></tr>
<tr><td>10</td><td>NRESET</td><td>Reset input pin, Active “L”.</td></tr>
<tr><td>11</td><td>VSYNC</td><td>Vertical sync signal in RGB I/F.</td></tr>
<tr><td>12</td><td>HSYNC</td><td>Horizontal sync signal in RGB I/F.</td></tr>
<tr><td>13</td><td>DOTCLK</td><td>Pixel clock signal in RGB I/F.</td></tr>
<tr><td>14</td><td>ENABLE</td><td>Data enable signal in RGB I/F mode</td></tr>
<tr><td>15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32</td><td>D17
D16
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0</td><td>18-bit parallel bi-directional data bus for MPU-Ⅰsystem:
8-bit I/F: DB [7:0] is used.
9-bit I/F: DB [8:0] is used.
16-bit I/F: DB [15:10] is used.
18-bit I/F: DB [17:0] is used.

18-bit parallel bi-directional data bus for MPU-Ⅱsystem:
8-bit I/F: DB [17:10] is used.
9-bit I/F: DB [17:9] is used.
16-bit I/F: DB [17:10] and DB [8:1] is used.
18-bit I/F: DB [17:0] is used.

18-bit input data bus for RGB I/F.
6-bit/pixel: DB[5:0] is used;
16-bit/pixel: DB[17:13]=R[4:0], DB[11:6]=G[5:0] and DB[5:1]=B[4:0];
18-bit/pixel: DB[17:12]=R[5:0], DB[11:6]=G[5:0] and DB[5:0]=B[5:0];
Connect unused pins to GND.</td></tr>
</table>

33	SDO	Serial output signal in SPI I/F.
34	SDI_SDA	Serial input signal in SPI I/F.
35	RDX	Reads strobe signal to write data when RDX is “Low” in MPU interface.
36	WRX_D/CX	MCU: Serves as a write signal and writes data at the rising edge. 4-line SPI: Serves as command or parameter select.
37	D/CX_SCL	Display data / command selection in 80-series MPU I/F. D/CX =”0”: Command D/CX =”1”: Display data. SPI: This pin is used serial interface clock in SPI.
38	CSX	Chip select input pin (“Low” enable) in MPU I/F and SPI I/F.
39	TE	Tearing effect output pin to synchronize MPU to frame writing.
40	IOVCC	I/O power supply.
41	IOVCC	I/O power supply.
42	VCI	System power supply.
43	GND	Power ground
44	NC	No connection
45	NC	
46	NC	
47	NC	
48	GND	Power ground
49	GND	Power ground
50	GND	Power ground

5. Absolute Maximum Ratings

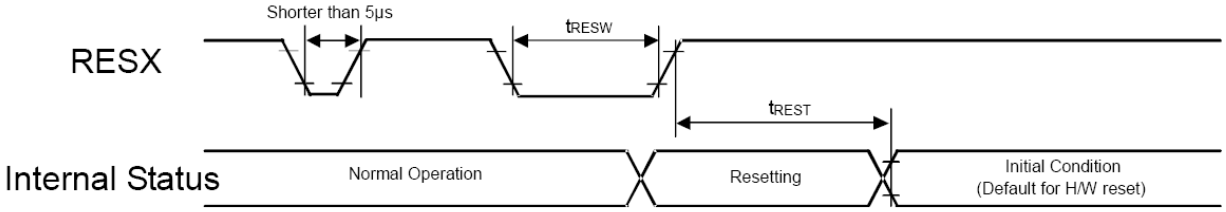
Item	Symbol	Min.	Max.	Unit
Logic Supply Voltage	IOVCC	-0.3	4.6	V
Analog Supply Voltage	VCI	-0.3	4.6	V
Input Voltage	Vin	-0.3	IOVCC+0.3	V
Operating Temperature	TOP	-20	70	°C
Storage Temperature	TST	-30	80	°C
Storage Humidity	HD	20	90	%RH

6. DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Logic Supply Voltage	IOVCC	1.65	1.8/2.8	3.3	V	-
Analog Supply Voltage	VCI	2.5	2.8	3.3	V	-
Input High Voltage	V_{IH}	0.7IOVCC	-	IOVCC	V	Digital input pins
Input Low Voltage	V_{IL}	GND	-	0.3IOVCC	V	Digital input pins
Output High Voltage	V_{OH}	0.8IOVCC	-	IOVCC	V	Digital output pins
Output Low Voltage	V_{OL}	GND	-	0.2IOVCC	V	Digital output pins
I/O Leak Current	I_{LI}	-0.1	-	0.1	uA	-

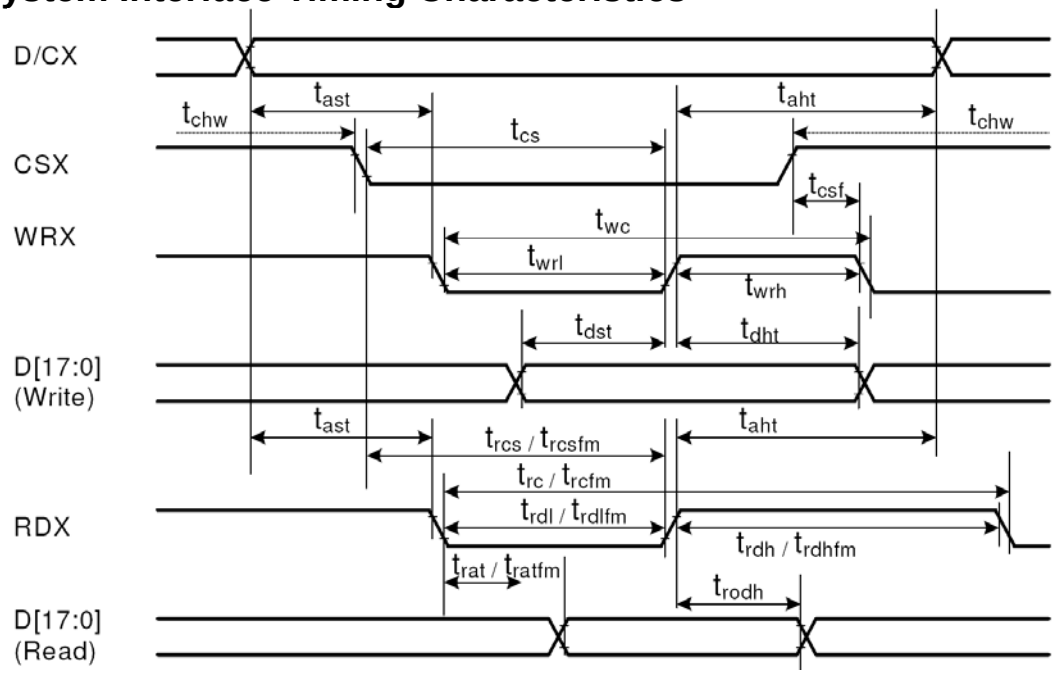
7. Timing Characteristics

7.1 Reset Timing Characteristics



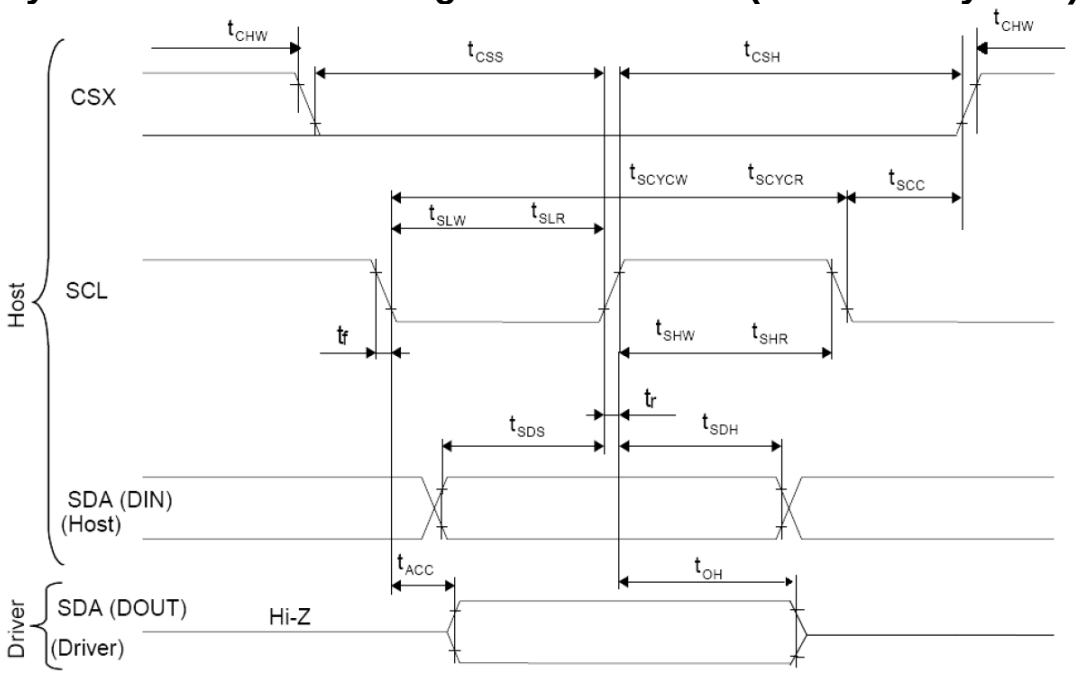
Symbol	Parameter	Related pins	Min.	Typ.	Max.	Note	Unit
t_{RESW}	Reset low pulse width(1)	RESX	10	-	-	-	µs
t_{REST}	Reset complete time(2)	-	5	-	-	When reset is applied during Sleep In mode	ms
		-	120	-	-	When reset is applied during Sleep Out mode	ms

7.2 i80-System Interface Timing Characteristics



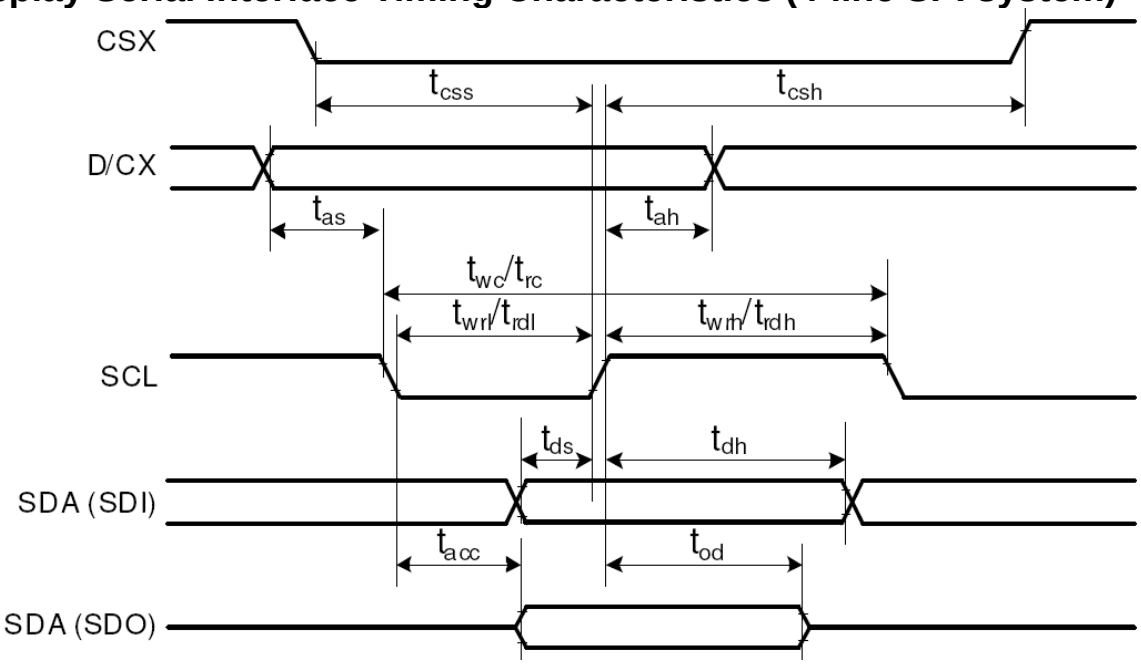
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

7.3 Display Serial Interface Timing Characteristics (3-line SPI system)



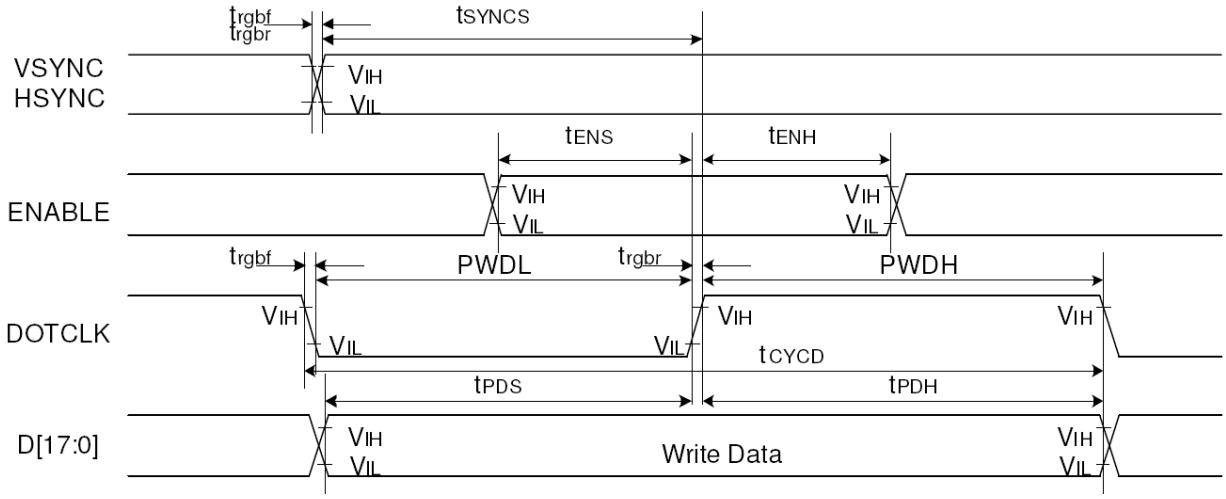
Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL “H” Pulse Width (Write)	40	-	ns	
	tslw	SCL “L” Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL “H” Pulse Width (Read)	60	-	ns	
	tslr	SCL “L” Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX “H” Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

7.4 Display Serial Interface Timing Characteristics (4-line SPI system)



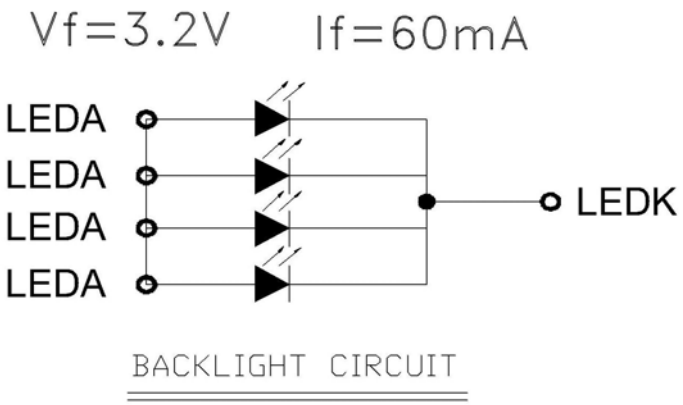
Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL “H” pulse width (Write)	40	-	ns	
	twrl	SCL “L” pulse width (Write)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL “H” pulse width (Read)	60	-	ns	
	trdl	SCL “L” pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

7.5 Parallel 24/18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

8. Backlight Characteristics



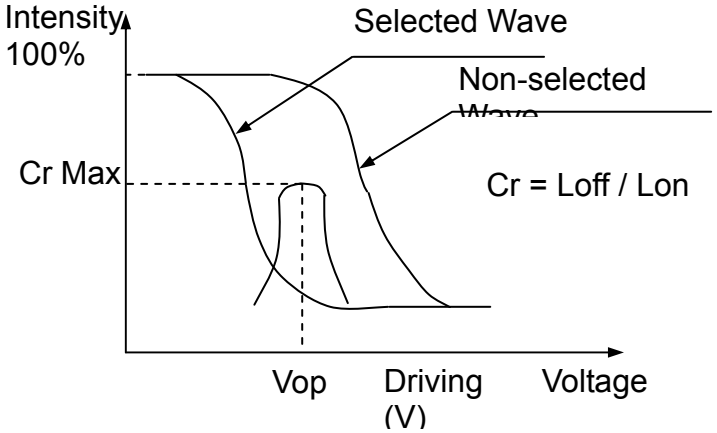
BACKLIGHT CIRCUIT

Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition
Supply Voltage	Vf	2.9	3.2	3.5	V	If=60mA
Supply Current	If	--	60	80	mA	--
Luminous Intensity for LCM	--	180	230	--	Cd/m^2	If=60mA
Uniformity for LCM	--	80	--	--	%	If=60mA
Life Time	--	50000	--	--	Hr	If=60mA
Backlight Color	White					

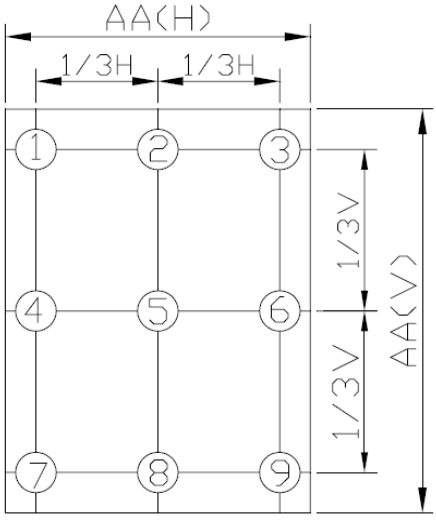
9. Optical Characteristics

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
Brightness		BL	θ =φ= 0°	180	230	--	cd/m²	Note2
Contrast Ratio		CR	θ =φ= 0°	--	500	--	--	Note3
Response Time		Tr+ Tf	θ =φ= 0°	--	16	--	ms	Note4
Viewing Angle	Upper	θ	CR≧10	--	50	--	--	Note 5
	Down			--	20	--	--	
	Right	φ		--	45	--	--	
	Left			--	45	--	--	
Color Filter Chromaticity	White	X	θ =φ= 0°	0.22	0.27	0.32	--	Note 6
		y		0.24	0.29	0.34	--	
	Red	X	θ =φ= 0°	0.57	0.62	0.67	--	
		y		0.28	0.33	0.38	--	
	Green	X	θ =φ= 0°	0.26	0.31	0.36	--	
		y		0.51	0.56	0.61	--	
	Blue	X	θ =φ= 0°	0.06	0.11	0.16	--	
		y		0.03	0.08	0.13	--	

Note1: Definition of Operation Voltage (Vop)

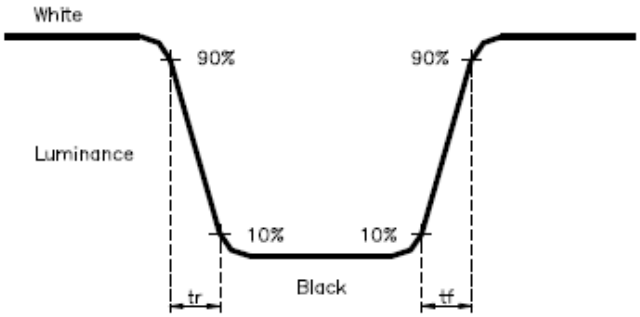


Note2: Definition of Luminance Uniformity：L = L(MIN) / L (MAX) × 100%

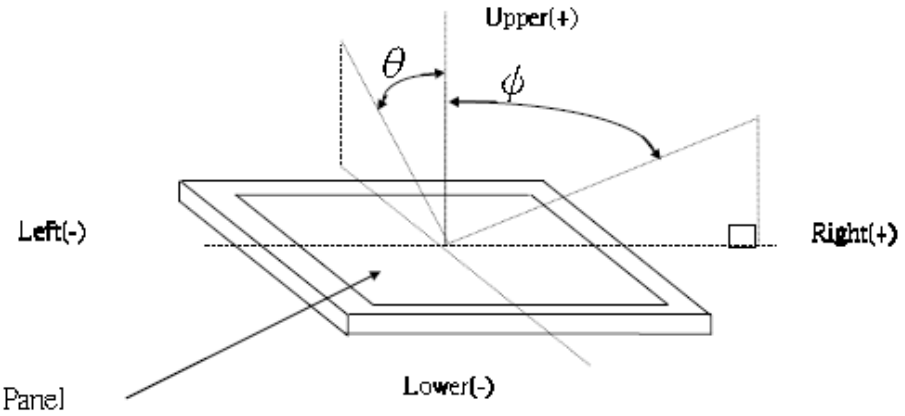


Note 3. Definition of Contrast Ratio：
CR = White Luminance (ON) / Black Luminance (OFF)

Note 4. Definition of response time：The response time is defined as the time interval between the 10% and 90% amplitudes.



Note 5. Definition of view angle(θ，ψ)：



Note 6. Light source: C light.

10. Reliability Test Conditions and Methods

NO.	TEST ITEMS	TEST CONDITION	INSPECTION AFTER TEST
□	High Temperature Storage	80°C±2°C×200Hours	Inspection after 2~4hours storage at room temperature, the samples should be free from defects: 1, Air bubble in the LCD. 2, Seal leak. 3, Non-display. 4, Missing segments. 5, Glass crack. 6, Current IDD is twice higher than initial value. 7, The surface shall be free from damage. 8, The electric characteristic requirements shall be satisfied.
□	Low Temperature Storage	-30°C±2°C×200Hours	
□	High Temperature Operating	70°C±2°C×120Hours	
□	Low Temperature Operating	-20°C±2°C×120Hours	
□	Temperature Cycle(Storage)	-20°C (30min) ⟺ 25°C (5min) ⟺ 70°C (30min) 1cycle Total 10cycle	
□	Damp Proof Test (Storage)	50°C±5°C×90%RH×120Hours	
□	Vibration Test	Frequency:10Hz~55Hz~10Hz Amplitude:1.5M X,Y,Z direction for total 3hours (Packing Condition)	
□	Drooping Test	Drop to the ground from 1M height one time every side of carton. (Packing Condition)	
□	ESD Test	Voltage:±8KV,R:330Ω,C:150PF,Air Mode,10times	

REMARK:
1, The Test samples should be applied to only one test item.
2, Sample side for each test item is 5~10pcs.
3,For Damp Proof Test, Pure water(Resistance＞10MΩ)should be used.
4,In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
5, EL evaluation should be accepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.
6, Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

11. Inspection Standard

This standard apply to C-STN/TFT module

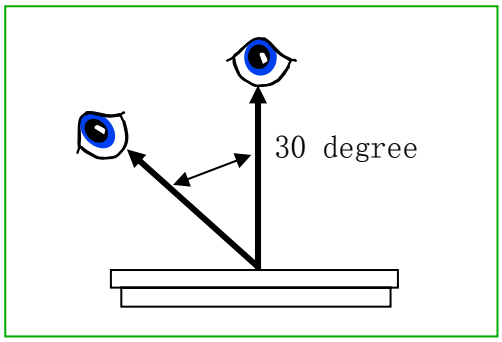
1. **Spot check plan：**

According to spot check level Ⅱ,MIL-STD-105D Level Ⅱ,the rank of accept or reject is below:

3A 级、2A 级 : major non-conformance : AQL 0.25 minor non-conformance : AQL 0.4

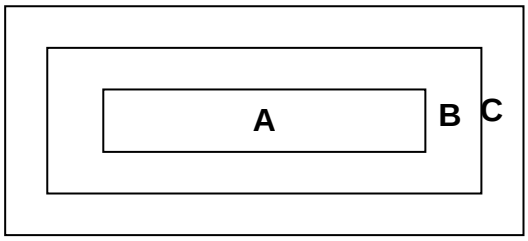
A 级：major non-conformance： AQL 0.65 minor non-conformance： AQL 1.

2. **Inspection condition：**



Under daylight lamp 20～40W，product distance inspector ‘eye 30cm,incline degree 30°。

3. **LCD area define：**



Area A：display area

Area B：VA area

Area C：out of VA area, not in sight after assembly

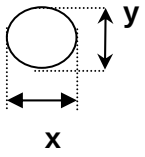
Remark: non-conformance at area C, but is OK that isn’t influence reliability of product & assembly by customer.

4. Inspection standard

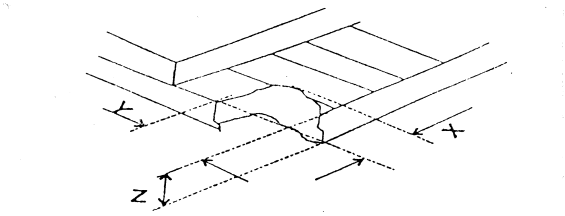
4.1 Major non-conformance

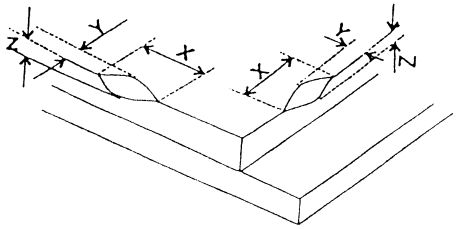
NO.	Item	Inspection standard	Rate
4.1.1	Function non-conformance	1) No display, display abnormally 2) Miss line, short 3) B/L no function or function abnormally 4) TP no function	major
4.1.2	miss	No matter miss what component	
4.1.3	Out of size	Module dimension out of spec	

4.2 Appearance non-conformance

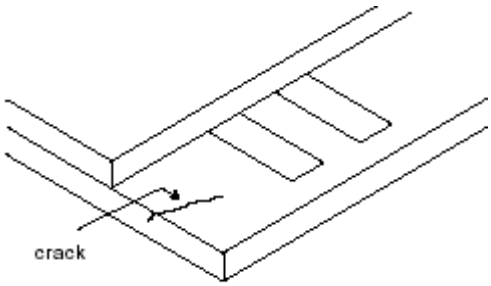
<table>
<tr><th>NO.</th><th>Item</th><th>Inspection standard</th><th>Rate</th></tr>
<tr><td>4.2.1</td><td>Black or white spot（power on）</td><td>
dot non-conformance define Φ
$\Phi = \frac{(x+y)}{2}$


A grade
<table>
<tr><th rowspan="2">Area
Size (mm)</th><th colspan="3">Most approve q’ty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.10</td><td colspan="2">ignore</td><td rowspan="5">ignore</td></tr>
<tr><td>0.10＜Φ≤0.15</td><td colspan="2">3</td></tr>
<tr><td>0.15＜Φ≤0.20</td><td colspan="2">2</td></tr>
<tr><td>0.20＜Φ≤0.25</td><td colspan="2">1</td></tr>
<tr><td>0.25＜Φ</td><td colspan="2">0</td></tr>
</table>
Most approve 4 damages, dot to dot ⩾10mm
</td><td>Minor</td></tr>
</table>

<table>
<tr>
<td>4.2.2</td>
<td>Black or white line（power on）</td>
<td>A grade
<table>
<tr><th colspan="2">Size(mm)</th><th colspan="3">Most approve q’ty</th></tr>
<tr><th>L(length)</th><th>W(width)</th><th>A</th><th>B</th><th>C</th></tr>
<tr><td>ignore</td><td>W≤0.03</td><td colspan="2">ignore</td><td rowspan="4">ignore</td></tr>
<tr><td>L≤5.0</td><td>0.03＜W≤0.05</td><td colspan="2">2</td></tr>
<tr><td>L≤3.0</td><td>0.05＜W≤0.07</td><td colspan="2">1</td></tr>
<tr><td></td><td>0.07＜W</td><td colspan="2">Treat with dot non-conformance</td></tr>
</table>
Most approve 3 damages, line to line ⩾10mm</td>
<td>Minor</td>
</tr>
<tr>
<td>4.2.3</td>
<td>Polarizer position</td>
<td>1) Polarizer attach meet drawing, disallow out of LCD.
2) Polarizer must cover display area （special require unless）</td>
<td>Minor</td>
</tr>
<tr>
<td>4.2.4</td>
<td>LCD non-conformance</td>
<td>(i) crash at side（remark: S=ITO length）
 

<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>⩽3.0</td><td>⩽S</td><td>ignore</td></tr>
</table>
Crash disallow extend to ITO or seal.
(ii) commonly surface scathe
 

<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>⩽2.0</td><td><frame edge</td><td>ignore</td></tr>
</table></td>
<td>Minor</td>
</tr>
</table>

		(iii) crack **Disallow extend crack**  	
4.2.5	**Contrast voltage warp**	**VOP/Vlcd voltage of confirmed sample±0.15V**	**Minor**
4.2.6	**color**	**Color & luminance of module scope reference spec**	**Minor**
4.2.7	**Cross talk**	**Reference confirmed limit sample**	**Minor**

12. Handling Precautions

12.1 Mounting method

The LCD panel of AMSON TFT module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.

Extreme care should be needed when handling the LCD modules.

12.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent

[Recommended below] and wipe lightly

- Isopropyl alcohol
- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns

Do not use the following solvent on the pad or prevent it from being contaminated:

- Soldering flux
- Chlorine (Cl) , Sulfur (S)

If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happen by miss-handling or using some materials such as Chlorine (Cl), Sulfur (S) from customer, Responsibility is on customer.

12.3 Caution against static charge

The LCD module use C-MOS LSI drivers, so we recommended that you:

Connect any unused input terminal to VDD or GND, do not input any signals before power is turned on, and ground your body, work/assembly areas, and assembly equipment to protect against static electricity.

12.4 packing

- Module employs LCD elements and must be treated as such.
- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity

12.5 Caution for operation

- It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.
- An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.
- Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD's how dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- Slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

Usage under the maximum operating temperature, 50%Rh or less is required.

12.6 storing

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

- Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.
- Storing with no touch on polarizer surface by the anything else.
  [It is recommended to store them as they have been contained in the inner container at the time of delivery from us.

12.7 Safety

- It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.

13. Precaution for Use

13.1

A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

13.2

On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.

- When a question is arisen in this specification.
- When a new problem is arisen this is not specified in this specification.
- When an inspection specifications change or operating condition change in customer is reported to AMSON TFT and some problem is arisen in this specification due to the change.
- When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.

14. Packing Method

TBD