OLED 128RGBx128 (1.5")
Display Module

Product Specification

Part Name: OLED Display Module (1.5")
Part ID: CY-3051
Doc No.: SCY-3051-M-XX-V02

Customer:
Approved By:
Date:

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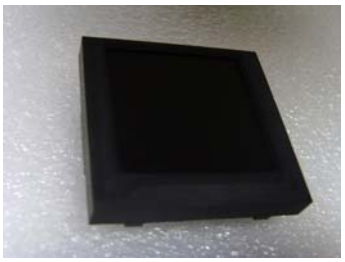
Record of Reversion

Rev	Issued Date	Description
V1.0	12/19/2008	New Create

1. Features


- Display Type: OLED 1.5”
- High Contrast / High Brightness/ Wide View Angle
- Single Power / Built in DC to DC Converter for OEL Panel
- Plastic Cover for Assembly easily
- Support Parallel & Serial Interface

2. General Specification

2.1. Display Specifications

- Display Mode : Passive Matrix
- Display Color : 262,144 Colors (Maximum)
- Drive Duty: 1/128 Duty
- Number of Pixels : 128(RGB) x 128
- Pixel Pitch: 0.07 x 0.21 mm
- Pixel Size: 0.045 x 0.194 mm
- View Angle: >160 Degree

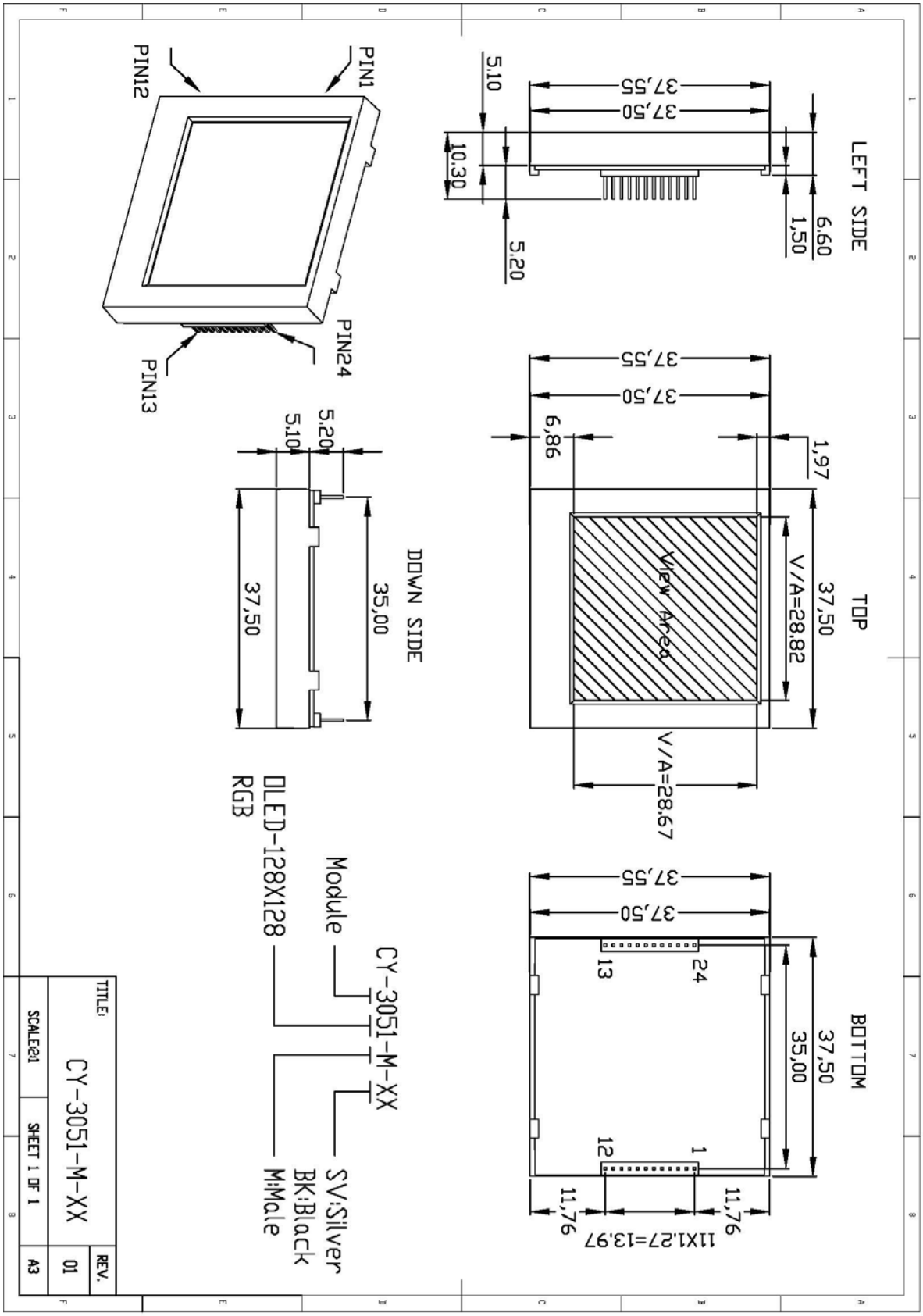
2.2. Mechanical Dimensions

- Dimensions : 37.50 x 37.50 x 10.30 mm
- Window Size : 28.660 x 28.664 mm
- Active Area: 26.855 x 26.864 mm
- Assembly: Pitch 1.27mm / 12 Pin Connector *2
- Assembly on PCB Easy & Removable & Flexible

2.3. Electrical Characteristic

- Supply Voltage: 2.4~3.5V
- Single Voltage Control Display Module
- Built-in DC to DC Power Supply to Drive OLED
- Driver IC: SSD1351
- Interface: Parallel/ Serial/ 68xx/ 80xx/ 4-wire SPI/ I^2C

3. Mechanical Drawing



4. Pin Assignments

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Type</th><th>Function</th></tr>
<tr><td>1</td><td>VDD</td><td>P</td><td>Power Supply for Core VDD
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>2</td><td>VSS</td><td>P</td><td>Ground for System
This is a ground pin. It must be connected to external source.</td></tr>
<tr><td>3</td><td>NC</td><td>-</td><td>Reserved Pin</td></tr>
<tr><td>4</td><td>NC</td><td>-</td><td>Reserved Pin</td></tr>
<tr><td>5
6</td><td>BS1
BS2</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>BS1</td><td>BS2</td></tr>
<tr><td>3-wire SPI</td><td>1</td><td>0</td></tr>
<tr><td>4-wire SPI</td><td>0</td><td>0</td></tr>
<tr><td>68XX-parallel (8-bit)</td><td>1</td><td>1</td></tr>
<tr><td>80XX-parallel (8-bit)</td><td>0</td><td>1</td></tr>
</table></td></tr>
<tr><td>7</td><td>CS#</td><td>I</td><td>Chip Select
This is the chip select input. The chip is enable for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>8</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Drive
This is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>9</td><td>D/C#</td><td>I</td><td>Data/ Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D0~D7 is treated as display data. When the pin is pulled low, the input at D0~D7 will be transferred to the command register.</td></tr>
<tr><td>10</td><td>WR#
(R/W#)</td><td>I</td><td>Write or Read/Write Select
When 80xx interface mode is selected, the pin will be the Write (WR#) input.
When interfacing to a 68xx-series microprocessor, the pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode.</td></tr>
<tr><td>11</td><td>RD#(E)</td><td>I</td><td>Read or Read/Write Enable
When 80xx interface mode is selected, the pin will be the Read (RD#) input.
When interfacing to a 68xx-series microprocessor, the pin will be used as the Enable (E) signal. Read/Write operation is initiated when this pin is pulled high and the CS# is pulled low.</td></tr>
<tr><td>12</td><td>NC</td><td>-</td><td>Reserved Pin</td></tr>
<tr><td>13~20</td><td>D0~D7</td><td>I/O</td><td>Host Data Input /Output Bus
These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to VSS except for D2.</td></tr>
<tr><td>21</td><td>VSS</td><td>P</td><td>Ground for System
This is a ground pin. It must be connected to external source.</td></tr>
<tr><td>22</td><td>VCC-CTL</td><td>I</td><td>OLED Driver Power Supply ON/ OFF Control
When this pin is pulled high, the panel power supply will be turned ON. When this pin is pulled low, the panel power supply will be turned OFF.</td></tr>
<tr><td>23</td><td>NC</td><td>-</td><td>Reserved Pin</td></tr>
<tr><td>24</td><td>VCC</td><td>P</td><td>OLED Driver Power Supply Output
This pin is OLED driver power supply output. When VCC-CTL is pulled high, the pin will be output about 13V voltage.</td></tr>
</table>

5. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Operation	V_{CI}	-0.3	4	V	1,2
Supply Voltage for Logic	V_{DD}	-0.5	2.75	V	1,2
Supply Voltage for I/O Pins	V_{DD}	-0.5	V_{CI}	V	1,2
Supply Voltage for Display	V_{CC}	-0.5	16	V	1,2
Operating Temperature	T_{OP}	-30	70	˚C	-
Storage Temperature	T_{STG}	-40	80	˚C	-

Note 1：All the above voltages are on the basis of “VSS = 0V”

Note 2：When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also for normal operations, it is desirable to use this module under the conditions according to Section 6 “Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

6. Electrical Characteristics

6.1. DC Characteristics

Characteristics	Symbol	Conditions	Min	TYP	Max	Unit
Supply Voltage for Operation	V_{CI}		2.4	2.8	3.5	V
Supply Voltage for Logic	V_{DD}		2.4	2.5	2.6	V
Supply Voltage for Display	V_{CC}	Note 1	12.5	13	13.5	V
High Level Input	V_{IH}		0.8×V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}		0	-	0.2x V_{DD}	V
High Level Output	V_{OH}	I_{out} = 100μA, 3.3MHz	0.9×V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}	I_{out} = 100μA, 3.3MHz	0	-	0.1x V_{DD}	V
Operating Current for V_{CI}	I_{CI}		-	240	300	μA
Operating Current for V_{CC}	I_{CC}	Note 2 Note 3	-	23.2 33.4	29.0 41.8	mA mA
Sleep Mode Current for V_{CI}	$I_{CI, SLEEP}$		-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	1	5	μA

Note 1: Brightness (L_{br}) and Supply Voltage for Display (Vcc) are subject to the change of the panel characteristics and the customer's request.

Note 2: V_{CI} = 2.8V, V_{CC} = 13V, 50% Display Area Turn on.

Note 3: V_{CI} = 2.8V, V_{CC} = 13V, 100% Display Area Turn on.

6.2. Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (White)	L_{br}	With Polarizer (Note 4)	70	90	-	cd/m^2
C.I.E. (White)	(x) (y)	With Polarizer	0.26 0.29	0.30 0.33	0.34 0.37	
C.I.E. (Red)	(x) (y)	With Polarizer	0.60 0.30	0.64 0.34	0.68 0.38	
C.I.E. (Green)	(x) (y)	With Polarizer	0.27 0.58	0.31 0.62	0.35 0.66	
C.I.E. (Blue)	(x) (y)	With Polarizer	0.10 0.12	0.14 0.16	0.18 0.20	
Dark Room Contrast	CR		-	>2000:1	-	
View Angle			>160	-	-	degree

* Optical measurement taken at V_{CI} = 2.8V, V_{CC} = 13V.

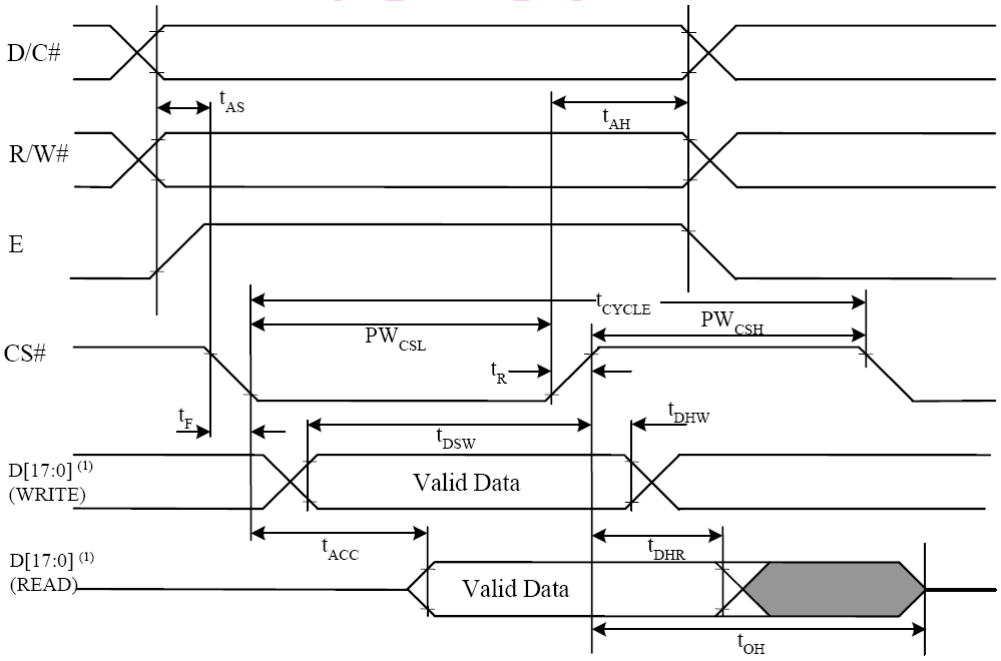
Note 4: Brightness (L_{br}) and Supply Voltage for Display (Vcc) are subject to the change of the panel characteristics and the customer's request.

7. Timing Chart

7.1. 68XX-Series MPU Parallel Interface Timing Characteristics

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	120 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* ($V_{DD} – V_{SS}$ = 2.4V to 2.6V, V_{DD} = 1.65V, V_{CI} = 2.8V, Ta = 25˚C)

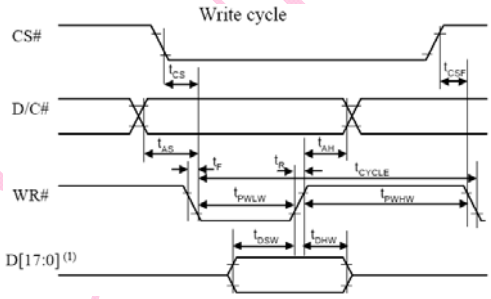


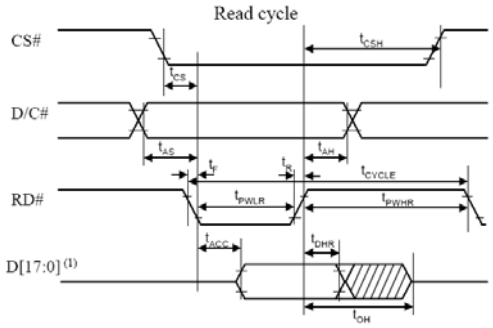
* When 8-bit Used: D[7:0] Instead

7.2. 80XX-Series MPU Parallel Interface Timing Characteristics

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{A8}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DD} = 1.65V, V_{CI} = 2.8V, Ta = 25˚C)



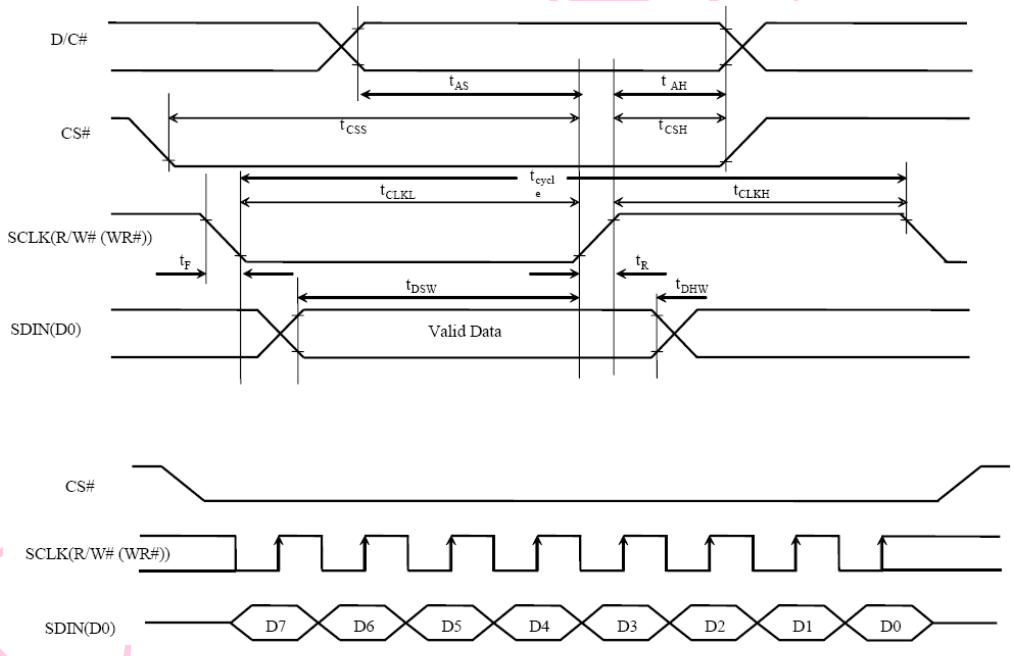


* When 8-bit Used: D[7:0] Instead

7.3. Series Interface Timing Characteristics (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

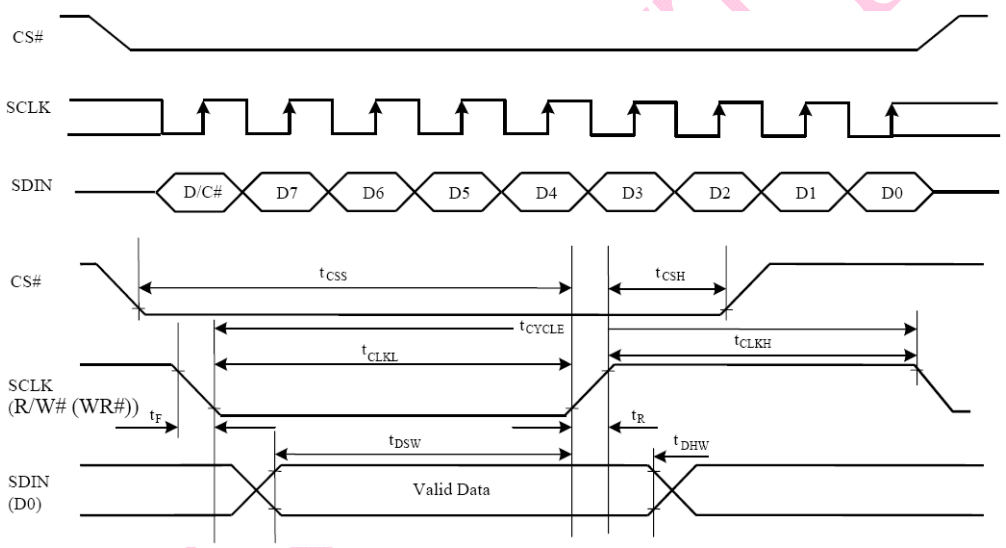
* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DD} = 1.65V, V_{CI} = 2.8V, Ta = 25°C)



7.4. Series Interface Timing Characteristics (3-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DD} = 1.65V, V_{CI} = 2.8V, Ta = 25°C)



8. Function Specification

8.1. Commands

Refer to the Technical Manual for the SSD1351

8.2. Power Down and Power up Sequence

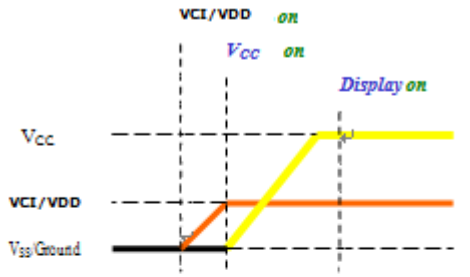
To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

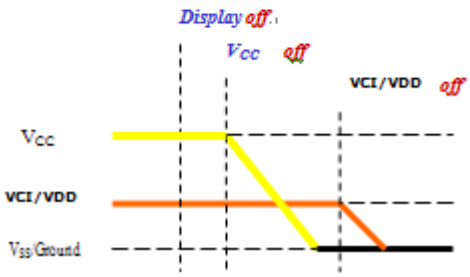
8.2.1. Power up Sequence

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (when V_{CC} is stable)
7. Send Display on command

8.2.2. Power down Sequence

1. Send Display off command
2. Power down Vcc
3. Delay 100ms
   (when Vcc is reach 0 and panel is completely discharges)
4. Power down V_{CI} & V_{DD}





8.3. Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128(RGB)×128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Command A2h, B1h, B3h, BBh, BEh are locked by command FDh

9. Command Application Example

Command usage and explanation of an actual example

<Initialization>

```
OLED_VCC_CTL=0;                 //Off power up Panel Vcc
OLED_RESET=0;                   //Reset driver IC for 100ms
Delay_100ms (1);
OLED_RESET=1;
Command Lock (0xFD, 0x12);
Command Lock (0xFD, 0xB1);
Set Sleep Mode On (0xAE);
Set Display bck Divide Ratio/ Oscillat or Frequency (0xB3, 0xF1);
Set Multiplex Ratio (0xCA, 0x7F);
Set Display Offset (0xA2, 0x00);
Set Display Start Line (0xA1, 0x00);
Set Re-Map & Color Depth (0xA0, 0xB4);
Set GPIO (0xB5, 0x00);
Function Selection (0xAB, 0x01);
Set Segment Low Voltage (0xB4, 0xA0, 0xB5, 0x55);
Set Contrast Current (0xC1, 0xC8, 0x80, 0xC8);
Set Master Current Control (0xC7, 0x0F);
Gamma Look up Table (0xB8, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, 0x09, 0x0A, 0x0B, 0x0C,
0x0D, 0x0E, 0x0F, 0x10, 0x11, 0x12, 0x13, 0x15, 0x17, 0x19, 0x1B, 0x1D, 0x1F, 0x21, 0x23, 0x25,
0x27, 0x2A, 0x2D, 0x30, 0x33, 0x36, 0x39,0x3C, 0x3F, 0x42, 0x45, 0x48, 0x4C, 0x50, ox54, 0x58,
0x5C, 0x60,x 0x64, ox68, 0x6C, 0x70,x 0x74, 0x78, 0x7D, 0x82, 0x87, 0x8C, 0x91, 0x96x
0x9B,0xA0, 0xA5, 0xAA, 0xAF, 0xB4);
Set Phase Length (0xB1, 0x32);
Enhance Driving Scheme Capability (0xB2, 0xA4, 0x00, 0x00);
Set Pre-Charge Voltage (0xBB, 0x17);
Set Second Pre-Charge Period (0xB6, 0x01);
Set VCOMH Voltage (0xBE, 0x05);
Set Display Mode (0xA6);
Clear Screen;
Set Sleep Mode Off (0xAF);
OLED_VCC=1;                     //Power up Vcc
Delay_100ms(1);                 //Dealy 100ms
Set_Display_On(0xAF);           // Display On (0x00/0x01)
```

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

10. Reliability

10.1. Contents of Reliability Test

Item	Conditions	Criteria
High Temperature Operation	70°C, 240hrs	The operational functions work.
Low Temperature Operation	-30°C, 240hrs	
High Temperature Storage	80°C, 240hrs	
Low Temperature Storage	-40°C, 240hrs	
High Temperature/ Humidity Operation	60°C, 90% RH, 120hrs	
Thermal Shock	-40°C <=> 85°C, 24 cycles 60 mins dwell	

*The samples used for the above test do not include polarizer.

*No moisture condensation is observed during tests.

10.2. Lifetime

End of lifetime is specified as 50% of initial brightness.

Parameter	Min	Max	Unit	Condition	Notes
Operating Life Time	10,000	-	hr	90 cd/m^2, 50% checkerboard	*
Storage Life Time	20,000	-	hr	Ta = 25°C, 50% RH	

*The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

10.3. Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23 ± 5°C；55 ± 15% RH.